Remarks

As stated above, the applicants appreciate the examiner's thorough examination of the subject application and request reexamination and reconsideration of the subject application in view of the preceding amendments and the following remarks.

Concerning Items 1-18 of the subject action, the Examiner rejects claims 1-2, 4-5, 6, 9-10, 12-14, 21-22, 24, 26-27 and 29, under 35 USC §102(a), based on the teachings of Movall et al. (U.S. Patent No. 6,101,557; hereinafter Movall).

Applicants claim (in currently amended claim 1):

> a system comprising: (a) a peripheral device adapted to define a plurality of device functions accessible through a data interface with a data bus, wherein at least one of the plurality of device functions is an external device function; (b) a first processing system adapted to communicate with a first device function defined by the peripheral device through the data interface; and (c) a second processing system adapted to communicate with a second device function defined by the peripheral device through the data interface. *Emphasis Added.*

Applicants claim (in currently amended claim 9):

> A method comprising: (a) initiating a first enumeration procedure at a first processing system to enumerate a first device function defined by a peripheral device coupled to a data interface of a data bus; and (c) initiating a second enumeration procedure at a second processing system to enumerate a second device function defined by the peripheral device; (c) wherein at least one of the first and second device functions is an external device function. *Emphasis Added.*

Applicants claim (in currently amended claim 21):

> 21. (Currently Amended) A processing system comprising: (a) logic to initiate a first enumeration procedure to enumerate a first device function defined by a peripheral device coupled to a data interface of a data bus, the peripheral device defining a plurality of device functions, wherein at least one of the plurality of device functions is an external device function; and (b) logic to initiate a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures while enabling the subsequent enumeration procedures to access at least one other device function defined by the peripheral device. *Emphasis Added.*

Applicants claim (in currently amended claim 26):

> 26. (Currently Amended) A method comprising: (a) initiating a first enumeration procedure at a first processing system to enumerate a first device function defined by a peripheral device coupled to a data interface of a data bus, the peripheral device defining a plurality of device functions, wherein at least one of the plurality of device functions is an external device function; and (b) initiating a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure. *Emphasis Added.*

Applicants respectfully assert that Movall fails to disclose elements (a) of applicants' claim 1, namely "a peripheral device adapted to define a plurality of device functions accessible through a data interface with a data bus, ***wherein at least one of the plurality of device functions is an external device function***". Further, applicants respectfully assert that Movall fails to disclose elements (c) of applicants' claim 9, namely "***wherein at least one of the first and second device functions is an external device function***". Additionally, applicants respectfully assert that Movall fails to disclose elements (a) of applicants' claim 21, namely "logic to initiate a first enumeration procedure to enumerate a first device function defined by a peripheral device coupled to a data interface of a data bus, the peripheral device defining a plurality of device functions, ***wherein at least one of the plurality of device functions is an external device function***". Further, applicants respectfully assert that Movall fails to disclose elements (a) of applicants' claim 26, namely "initiating a first enumeration procedure at a first processing system to enumerate a first device function defined by a peripheral device coupled to a data interface of a data bus, the peripheral device defining a plurality of device functions, ***wherein at least one of the plurality of device functions is an external device function***".

Accordingly, applicants respectfully assert that Movall is not a proper basis for a 35 USC §102(a) rejection, as the reference fails to disclose each and every element of the applicants' claimed invention.

Concerning the "plurality of device functions" claimed by the applicants, the applicants disclose that:

> An "I/O channel" as referred to herein relates to an entity through which data may be transmitted to, or received from an external system. For example, an I/O channel may comprise a peripheral device or device function to transmit data between a data bus and a communication or storage device. However, this is

> merely an example of an I/O channel and embodiments of the present invention are not limited in this respect. *See the subject application, paragraph 25.*

Further, applicants disclose that:

> the I/O processor 14 and host processing system 12 may each execute an enumeration procedure to configure resources to communicate with one or more of the devices functions associated with the I/O channels 20 and 22. *See the subject application, paragraph 30.*

Accordingly, I/O channels 20, 22 are entities through which data is received from or transmitted to an external system.

Concerning the teaching of Movall, Movall discloses that:

> The function routing/control facility 400 is located in the multifunction device 260 and routes data and/or control signals between the I/O device driver 140 and the I/O device adapters 250-0 to 250-n which correspond in number to the number of I/O devices 280-n connected to the multi-function device 260. The function routing/control facility 400 includes a function configuration register 420, controller configuration register 430 and a slot owner configuration register 440. *See Movall, column 5, lines 4-19.*

Further, Movall discloses that:

> In the example of FIG. 2, the processor complex 100 via the PCI device driver 140 is the host unit. However, as will be illustrated in further detail with respect to FIGS. 3 and 4, the slot owner configuration register can be updated for a given slot 0 to n to indicate that that slot is owned by one of the other slots of the PCI multi-function device 260.
>
> In the example where function 0 is an intelligent I/O adapter or controller of functions 1,2, then the host processor, the processor complex 100 of FIG. 2, does not actually see functions 1 and 2, but rather sees only function 0, the location of the intelligent I/O adapter or controller. *See Movall, column 6, lines 33-44.*

However, the functions of Movall (See Movall, FIG. 2B, Items 250-0 through 250-N) are all local functions and, therefore, are not equivalent to the functions (e.g., I/O channels 20 and 22) disclosed and claimed by the applicants. Hence, Movall fails to disclose a system in which "at least one of the plurality of device functions is an external device function"

Accordingly, applicants respectfully assert that Movall is not a proper basis for a 35 USC §102(a) rejection, as the reference fails to disclose each and every element of applicants'

currently amended claims 1, 9, 21 and 26. Therefore, the applicants respectfully assert that independent claims 1, 9, 21 and 26 are patentable over the cited reference.

Further, as dependent claims 2-8 depend (either directly or indirectly) upon independent claim 1, applicants respectfully assert that claims 2-8 are also patentable over the cited reference. Additionally, as dependent claims 10-16 depend (either directly or indirectly) upon independent claim 9, applicants respectfully assert that claims 10-16 are also patentable over the cited reference. Further, as dependent claims 22-25 depend (either directly or indirectly) upon independent claim 21, applicants respectfully assert that claims 22-25 are also patentable over the cited reference. Finally, as dependent claims 27-29 depend (either directly or indirectly) upon independent claim 26, applicants respectfully assert that claims 27-29 are also patentable over the cited reference.

Concerning Items 19-27 of the subject action, the Examiner rejects claims 1-2, 4-5, 9-10 and 12-13, under 35 USC §102(a), based on the teachings of Emerson et al. (U.S. Patent No. 6,212,587; hereinafter Emerson).

Applicants claim (in currently amended claim 1):

> a system comprising: (a) a peripheral device adapted to define a plurality of device functions accessible through a data interface with a data bus, wherein at least one of the plurality of device functions is an external device function; (b) a first processing system adapted to communicate with a first device function defined by the peripheral device through the data interface; and (c) a second processing system adapted to communicate with a second device function defined by the peripheral device through the data interface. *Emphasis Added.*

Applicants claim (in currently amended claim 9):

> A method comprising: (a) initiating a first enumeration procedure at a first processing system to enumerate a first device function defined by a peripheral device coupled to a data interface of a data bus; and (c) initiating a second enumeration procedure at a second processing system to enumerate a second device function defined by the peripheral device; (c) wherein at least one of the first and second device functions is an external device function. *Emphasis Added.*

Applicants respectfully assert that Emerson fails to disclose elements (a) of applicants' claim 1, namely "a peripheral device adapted to define a plurality of device functions accessible through a data interface with a data bus, ***wherein at least one of the plurality of device functions is an external device function***". Further, applicants respectfully assert that Movall fails to

disclose elements (c) of applicants' claim 9, namely "***wherein at least one of the first and second device functions is an external device function***".

Accordingly, applicants respectfully assert that Emerson is not a proper basis for a 35 USC §102(a) rejection, as the reference fails to disclose each and every element of the applicants' claimed invention.

Concerning the teaching of Emerson, Emerson discloses that:

> The PCI bus segment 200 typically includes one or more non-hidden peripheral devices 240 connected to the PCI bus 230 which are not hidden from the host CPUs 250. The non-hidden peripheral devices 240 can be any computing device including, but not limited to, video graphics adapters, LAN interfaces, SCSI bus adapters, and mass storage devices, such as disk drive assemblies. Memory space for storing information pertaining to each of the non-hidden peripheral devices 240 is accessible by the host CPUs 250. Therefore, the host CPUs 250 can detect the presence of the non-hidden peripheral devices 240 and can access them directly without intervention of an IOP 290.
>
> The PCI bus segment 200 also includes one or more hidden peripheral devices 270 connected to the PCI bus 230 which are hidden from the host CPUs 250. The hidden peripheral devices 270 also include, but are not limited to, video graphics adapters, LAN interfaces, SCSI bus adapters, and mass storage devices, such as disk drive assemblies. Memory space for storing information pertaining to each of the hidden peripheral devices 270 is inaccessible by the host CPUs 250 and, therefore, the host CPUs 250 are unable to detect the presence of the hidden peripheral devices 270 and cannot access them directly without the intervention of the IOP 290. *See Emerson, column 4, lines 6-29.*

As with Movall, the functions of Emerson (See Emerson, FIG. 1, Items 240, 270) are all local functions and, therefore, are not equivalent to the functions (e.g., I/O channels 20 and 22) disclosed and claimed by the applicants. Hence, Emerson fails to disclose a system in which "at least one of the plurality of device functions is an external device function"

Accordingly, applicants respectfully assert that Emerson is not a proper basis for a 35 USC §102(a) rejection, as the reference fails to disclose each and every element of applicants' currently amended claims 1 and 9. Therefore, the applicants respectfully assert that independent claims 1 and 9 are patentable over the cited reference.

Further, as dependent claims 2-8 depend (either directly or indirectly) upon independent claim 1, applicants respectfully assert that claims 2-8 are also patentable over the cited reference.

Additionally, as dependent claims 10-16 depend (either directly or indirectly) upon independent claim 9, applicants respectfully assert that claims 10-16 are also patentable over the cited reference.

Concerning Items 28-33 of the subject action, the Examiner rejects claims 3, 11, 23 and 28, under 35 USC §103(a), based on the combination of the teachings of Movall and Pecone et al. (U.S. Patent No. 6,044,207; hereinafter Pecone).

For the reasons discussed above, the applicants respectfully assert that independent claims 1, 9, 21 and 26 are patentable over Movall. As dependent claim 3 depends (either directly or indirectly) upon independent claim 1, dependent claim 11 depends (either directly or indirectly) upon independent claim 9, dependent claim 23 depends (either directly or indirectly) upon independent claim 21, and dependent claim 28 depends (either directly or indirectly) upon independent claim 26, the applicants respectfully assert that claims 3, 11, 23 and 28 are also patentable over the combination of the cited references.

Concerning Items 34-38 of the subject action, the Examiner rejects claims 7-8 and 15-16, under 35 USC §103(a), based on the combination of the teachings of Movall and Garbus et al. (U.S. Patent No. 5,734,847; hereinafter Garbus).

For the reasons discussed above, the applicants respectfully assert that independent claims 1 and 9 are patentable over Movall. As dependent claims 7-8 depend (either directly or indirectly) upon independent claim 1, and dependent claim 15-16 depend (either directly or indirectly) upon independent claim 9, the applicants respectfully assert that claims 7-8 and 15-16 are also patentable over the combination of the cited references.

Concerning Items 39-42 of the subject action, the Examiner rejects claims 17-18 and 20, under 35 USC §103(a), based on the combination of the teachings of Movall and Belser et al. (U.S. Patent No. 5,737,344; hereinafter Belser).

Applicants claim (in currently amended claim 17):

> 17. (Currently Amended) An article comprising: (a) storage medium comprising machine-readable instructions stored thereon for: (b) initiating a first enumeration procedure at a first processing system to enumerate a first device function defined by a peripheral device coupled to a data interface of a data bus, the peripheral device defining a plurality of device functions, wherein at least one of the plurality of device functions is an external device function; and (c) initiating a bus transaction on the data bus to cause the first device function to be

> concealed from subsequent enumeration procedures while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure. *Emphasis Added.*

Applicants respectfully assert that the combination of the teachings of Movall and Belser fails to disclose elements (b) of applicants' claim 17, namely "initiating a first enumeration procedure at a first processing system to enumerate a first device function defined by a peripheral device coupled to a data interface of a data bus, the peripheral device defining a plurality of device functions, ***wherein at least one of the plurality of device functions is an external device function***".

Accordingly, applicants respectfully assert that the combination of the teachings of Movall and Belser is not a proper basis for a 35 USC §103(a) rejection, as the combination fails to disclose each and every element of the applicants' claimed invention.

Specifically, the Examiner acknowledges that "Movall does not teach a storage medium comprising machine-readable instructions". Accordingly, the Examiner merely relies on Belser to disclose a "processor that executes machine-readable instructions stored on a direct access storage device".

In conjunction with the reasons discussed above, the applicants respectfully assert that independent claim 17 is patentable over the combination of Movall and Belser. As dependent claims 18 and 20 depend (either directly or indirectly) upon independent claim 17, the applicants respectfully assert that claims 18 and 20 are also patentable over the combination of the cited references.

Concerning Items 43-44 of the subject action, the Examiner rejects claim 19, under 35 USC §103(a), based on the combination of the teachings of Movall and Pecone.

For the reasons discussed above, the applicants respectfully assert that independent claim 17 is patentable over the combination of Movall and Belser. As dependent claim 19 depends (either directly or indirectly) upon independent claim 17, the applicants respectfully assert that claim 19 is also patentable over the combination of the cited references.

Concerning Items 45-46 of the subject action, the Examiner rejects claim 25, under 35 USC §103(a), based on the combination of the teachings of Movall and Wilson (U.S. Patent No. 5,960,213; hereinafter Wilson).

For the reasons discussed above, the applicants respectfully assert that independent claim 21 is patentable over Movall. As dependent claim 25 depends (either directly or indirectly) upon independent claim 21, the applicants respectfully assert that claim 25 is also patentable over the combination of the cited references.

Concerning Items 47-49 of the subject action, the Examiner rejects claims 3 and 11, under 35 USC §103(a), based on the combination of the teachings of Emerson and Pecone.

For the reasons discussed above, the applicants respectfully assert that independent claims 1 and 9 are patentable over Emerson. As dependent claim 3 depends (either directly or indirectly) upon independent claim 1, and dependent claim 11 depends (either directly or indirectly) upon independent claim 9, the applicants respectfully assert that claims 3 and 11 are also patentable over the combination of the cited references.

Concerning Items 50-52 of the subject action, the Examiner rejects claims 6 and 14, under 35 USC §103(a), based on the combination of the teachings of Emerson and Sutoh (U.S. Patent No. 6,678,770; hereinafter Sutoh).

For the reasons discussed above, the applicants respectfully assert that independent claims 1 and 9 are patentable over Emerson. As dependent claim 6 depends (either directly or indirectly) upon independent claim 1, and dependent claim 14 depends (either directly or indirectly) upon independent claim 9, the applicants respectfully assert that claims 6 and 14 are also patentable over the combination of the cited references.

Concerning Items 53-57 of the subject action, the Examiner rejects claims 7-8 and 15-16, under 35 USC §103(a), based on the combination of the teachings of Emerson and Garbus.

For the reasons discussed above, the applicants respectfully assert that independent claims 1 and 9 are patentable over Emerson. As dependent claims 7-8 depend (either directly or indirectly) upon independent claim 1, and dependent claims 15-16 depend (either directly or indirectly) upon independent claim 9, the applicants respectfully assert that claims 7-8 and 15-16 are also patentable over the combination of the cited references.

Concerning Items 58-60 of the subject action, the Examiner rejects claims 17-18, under 35 USC §103(a), based on the combination of the teachings of Emerson, Garbus and Belser.

Applicants claim (in currently amended claim 17):

> 17. (Currently Amended) An article comprising: (a) storage medium comprising machine-readable instructions stored thereon for: (b) initiating a first enumeration procedure at a first processing system to enumerate a first device function defined by a peripheral device coupled to a data interface of a data bus, the peripheral device defining a plurality of device functions, wherein at least one of the plurality of device functions is an external device function; and (c) initiating a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure. *Emphasis Added.*

Applicants respectfully assert that the combination of the teachings of Emerson, Garbus and Belser fails to disclose elements (b) of applicants' claim 17, namely "initiating a first enumeration procedure at a first processing system to enumerate a first device function defined by a peripheral device coupled to a data interface of a data bus, the peripheral device defining a plurality of device functions, ***wherein at least one of the plurality of device functions is an external device function***".

Accordingly, applicants respectfully assert that the combination of the teachings of Emerson, Garbus and Belser is not a proper basis for a 35 USC §103(a) rejection, as the combination fails to disclose each and every element of the applicants' claimed invention.

Specifically, the Examiner acknowledges that "Emerson does not teach initiating a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure; and a storage medium comprising machine-readable instructions". Accordingly, the Examiner relies on Garbus to disclose "initiating a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure". Further, the Examiner merely relies on Belser to disclose a "processor that executes machine-readable instructions stored on a direct access storage device".

In conjunction with the reasons discussed above, the applicants respectfully assert that independent claim 17 is patentable over the combination of Emerson, Garbus and Belser. As dependent claim 18 depends (either directly or indirectly) upon independent claim 17, the

applicants respectfully assert that claim 18 is also patentable over the combination of the cited references.

Concerning Items 61-62 of the subject action, the Examiner rejects claim 19, under 35 USC §103(a), based on the combination of the teachings of Emerson, Garbus, Belser and Pecone.

For the reasons discussed above, the applicants respectfully assert that independent claim 17 is patentable over the combination of the teachings of Emerson, Garbus and Belser. As dependent claim 19 depends (either directly or indirectly) upon independent claim 17, the applicants respectfully assert that claim 19 is also patentable over the combination of the cited references.

Concerning Items 63-64 of the subject action, the Examiner rejects claim 20, under 35 USC §103(a), based on the combination of the teachings of Emerson, Garbus, Belser and Kamepalli (U.S. Patent No. 6,647,434; hereinafter Kamepalli).

For the reasons discussed above, the applicants respectfully assert that independent claim 17 is patentable over the combination of the teachings of Emerson, Garbus and Belser. As dependent claim 20 depends (either directly or indirectly) upon independent claim 17, the applicants respectfully assert that claim 20 is also patentable over the combination of the cited references.

Concerning Items 65-69 of the subject action, the Examiner rejects claims 21-22 and 26-27, under 35 USC §103(a), based on the combination of the teachings of Emerson and Garbus.

Applicants claim (in currently amended claim 21):

> 21. (Currently Amended) A processing system comprising: (a) logic to initiate a first enumeration procedure to enumerate a first device function defined by a peripheral device coupled to a data interface of a data bus, the peripheral device defining a plurality of device functions, wherein at least one of the plurality of device functions is an external device function; and (b) logic to initiate a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures while enabling the subsequent enumeration procedures to access at least one other device function defined by the peripheral device. *Emphasis Added.*

Applicants claim (in currently amended claim 26):

> 26. (Currently Amended) A method comprising: (a) initiating a first enumeration procedure at a first processing system to enumerate a first device function defined by a peripheral device coupled to a data interface of a data bus, the peripheral device defining a plurality of device functions, wherein at least one of the plurality of device functions is an external device function; and (b) initiating a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure. *Emphasis Added.*

Applicants respectfully assert that the combination of Emerson and Garbus fails to disclose elements (a) of applicants' claim 21, namely "logic to initiate a first enumeration procedure to enumerate a first device function defined by a peripheral device coupled to a data interface of a data bus, the peripheral device defining a plurality of device functions, ***wherein at least one of the plurality of device functions is an external device function***". Further, applicants respectfully assert that the combination of Emerson and Garbus fails to disclose elements (a) of applicants' claim 26, namely "initiating a first enumeration procedure at a first processing system to enumerate a first device function defined by a peripheral device coupled to a data interface of a data bus, the peripheral device defining a plurality of device functions, ***wherein at least one of the plurality of device functions is an external device function***".

Accordingly, applicants respectfully assert that the combination of Emerson and Garbus is not a proper basis for a 35 USC §103(a) rejection, as the reference fails to disclose each and every element of the applicants' claimed invention.

Concerning claim 21, the Examiner acknowledges that "Emerson does not teach logic to initiate a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures while enabling the subsequent enumeration procedures to access at least one other device function defined by the peripheral device". Accordingly, the Examiner relies on Garbus to disclose "logic to initiate a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures while enabling the subsequent enumeration procedures to access at least one other device function defined by the peripheral device".

In conjunction with the reasons discussed above, the applicants respectfully assert that independent claim 21 is patentable over the combination of Emerson and Garbus. As dependent

claim 22 depends (either directly or indirectly) upon independent claim 21, the applicants respectfully assert that claim 22 is also patentable over the combination of the cited references.

Concerning claim 26, the Examiner acknowledges that "Emerson does not teach initiating a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure". Accordingly, the Examiner relies on Garbus to disclose "initiating a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure".

In conjunction with the reasons discussed above, the applicants respectfully assert that independent claim 26 is patentable over the combination of Emerson and Garbus. As dependent claim 27 depends (either directly or indirectly) upon independent claim 26, the applicants respectfully assert that claim 27 is also patentable over the combination of the cited references.

Concerning Items 70-72 of the subject action, the Examiner rejects claims 23 and 28 and 26-27, under 35 USC §103(a), based on the combination of the teachings of Emerson, Garbus and Pecone.

For the reasons discussed above, the applicants respectfully assert that independent claims 21 and 26 are patentable over the combination of Emerson and Garbus. As dependent claim 23 depends (either directly or indirectly) upon independent claim 21, and dependent claim 28 depends (either directly or indirectly) upon independent claim 26, the applicants respectfully assert that claims 23 and 28 are also patentable over the combination of the cited references.

Concerning Items 73-75 of the subject action, the Examiner rejects claims 24 and 29, under 35 USC §103(a), based on the combination of the teachings of Emerson, Garbus and Sutoh.

For the reasons discussed above, the applicants respectfully assert that independent claims 21 and 26 are patentable over the combination of Emerson and Garbus. As dependent claim 24 depends (either directly or indirectly) upon independent claim 21, and dependent claim 29 depends (either directly or indirectly) upon independent claim 26, the applicants respectfully assert that claims 24 and 29 are also patentable over the combination of the cited references.

Concerning Items 76-77 of the subject action, the Examiner rejects claim 25, under 35 USC §103(a), based on the combination of the teachings of Emerson, Garbus and Kamepalli.

For the reasons discussed above, the applicants respectfully assert that independent claims 21 is patentable over the combination of Emerson and Garbus. As dependent claim 25 depends (either directly or indirectly) upon independent claim 21, the applicants respectfully assert that claim 25 is also patentable over the combination of the cited references.

Concerning Item 78 of the subject action, the Examiner objects to the drawings for failing to illustrate the bridge of claims 4, 7 and 12. The applicant submits herewith a replacement drawing sheet that addresses the objection raised by the Examiner. No new subject matter has been added, as evidenced by the amended specification which discloses that:

> The I/O processor 14 comprises an internal bridge 19 which forms a primary bus 24 and a secondary bus 18. *See the subject application, paragraph 27.*

Concerning Item 80 of the subject action, the Examiner requests submission of a copy of the Information Disclosure Statement submitted 9 August 2004. In response to this request, the applicant submits herewith a copy of that Information Disclosure Statement.

No new matter has been added by these amendments. While the applicants respectfully assert that the subject application is now in condition for allowance, the Examiner is invited to telephone applicants' attorney (603-668-6560) to facilitate prosecution of this application. Please apply any charges or credits to deposit account 50-2121.

Respectfully submitted,

MARK A. SCHMISSEUR ET AL.

By their Representatives,

Grossman, Tucker, Perreault & Pfleger PLLC
c/o PortfolioIP
P.O. Box 52050
Minneapolis, MN 55402
603-668-6560

Date 1-24-05 By _____
Edmund P. Pfleger
Reg. No. 41,252

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 24 day of January, 2005.

MEREDITH MESCHER _____
Name Signature